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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/470,875
Filing Date: December 22, 1999
Appellant(s): KHAIRA ET AL.

Sumit Bhattacharya
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/3/06 appealing from the Office action mailed 10/24/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,339,836	Eisenhofer et al.	1-2002
6,175,946	Ly et al.	1-2001
6,108,494	Eisenhofer et al.	8-2000

5,881,270	Worthington et al.	3-1999
5,881,267	Dearth et al.	3-1999
5,732,247	Dearth et al.	3-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 4, 5, 7-10, 13-18, 21, 22, 24-27, 29, 30, 31, 32, 34-43, 45, 46, 48-51, and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenhofer et al. U.S. Patent 6,108,494 hereafter referred to as the *Eisenhofer–1* reference in view of Worthington et al. U.S. Patent 5,881,270 and in further view of Eisenhofer et al. U.S. Patent 6,339,836 hereafter referred to as the *Eisenhofer-2* reference.

As regards independent Claims 1, 21, 26, 29, 34 and 51 the *Eisenhofer-1* reference discloses a method for distributed simulation (Col. 7 Lines 15-25), at least two simulators (Figure 2), a back plane (Figure 2 Item 210), an interface for the simulators (Col. 5 Lines 52-67, Col. 6 Lines 1-20), fixed configuration back plane (Col. 5 Lines 5-7), exchanging messages (Col. 8 Lines 42-47) and data format conversions (Col. 5 Lines 52-67, Col. 6 Lines 1-20, Col. 12 Lines 34-67, Col. 13 Lines 1-5).

The *Eisenhofer-1* reference does not expressly disclose simulators that represent components of a system based on a processor and a chipset.

The *Worthington et al.* reference discloses a method for flexible simulation modeling that represent at least one of a component and a system based on processors and chipsets (Figures 1, 3, 3A, 4, Col. 4 Lines 47-61).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs *(Worthington et al. Col. 1 Lines 45-51).*

As regards the limitation of an apparatus in independent Claims 40 and 45 the *Eisenhofer-1* reference discloses an apparatus (Figure 3, Col. 6 Lines 46-67, Col. 7 Lines 1-25).

As regards independent Claims 53-55 the *Eisenhofer-1* reference discloses an articled with a storage medium wherein there is stored instructions for a processor (Figure 3, Col. 6 Lines 46-67, Col. 7 Lines 1-25).

As regards the limitation of validating a component/ element of a design in independent Claims 29, 34, 40 and 45 the *Eisenhofer-1* reference does not expressly disclose validation.

The *Worthington et al.* reference discloses validation (Col. 8 Lines 30-40).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs *(Worthington et al. Col. 1 Lines 45-51).*

As regards Claims 2, 22, 31, 38, 42 and 49 the *Eisenhofer-1* reference does not expressly disclose a driver.

The *Worthington et al.* reference discloses a driver (Figure 1 Item 14b).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs *(Worthington et al. Col. 1 Lines 45-51).*

As regards Claims 4, 24, 32, 39, 43, 50, the *Eisenhofer-1* reference does not expressly disclose generating specific circuit models, however the reference does discuss the use of models in circuit simulation.

The *Worthington et al.* reference discloses models of components used in circuit simulation (Figures 1-10, Col. 2 Lines 30-67, Col. 3 Lines 1-8).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs *(Worthington et al. Col. 1 Lines 45-51).*

As regards Claims 5, 25, 27, 30, 35, 41 and 46 the *Eisenhofer-1* reference discloses an integrated circuit (Col. 1 Lines 30-48).

As regards Claims 8, 9 and 56 the *Eisenhofer-1* reference discloses a global signal used for synchronization and simulators being relaxed based on the current state of that simulator (Col. 6 Lines 21-45).

As regards Claim 10 the *Eisenhofer-1* reference discloses synchronizing different types of simulators (Col. 11 Lines 60-67, Col. 12 Lines 1-25).

As regards Claims 13 and 15 the *Eisenhofer-1* reference discloses exchanging messages to enable simulators using different encoding schemes (Col. 5 Lines 52-67, Col. 6 Lines 1-20, Col. 12 Lines 34-67, Col. 13 Lines 1-5).

As regards Claims 14, 16 and 17 the *Eisenhofer-1* reference discloses resolving conflicts based on boundary conditions between different simulators (Figure 7, Col. 5 Lines 19-25, Col. 6 Lines 21-45, Col. 12 Lines 7-40).

As regards Claim 18 the *Eisenhofer-1* reference discloses high-level languages (Col. 7 Lines 27-51).

As regards Claims 37 and 48 the *Eisenhofer-1* reference does not expressly discloses a message from a second device.

The *Worthington et al.* reference discloses getting a test message from a second device (Figures 3, 4, 8, Col. 2 Lines 30-44).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component

models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs *(Worthington et al. Col. 1 Lines 45-51).*

Claims 3, 7, 20, 23, 28, 33, 36, 44, 47, are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenhofer et al. U.S. Patent 6,108,494 hereafter referred to as the *Eisenhofer–1* reference in view of Worthington et al. U.S. Patent 5,881,270 and in further view of Eisenhofer et al. U.S. Patent 6,339,836 hereafter referred to as the *Eisenhofer-2* reference and in further view of Ly et al. U.S. Patent 6,175,946.

As regards independent Claims 1, 21, 26, 29, and 34 see the rejection in this Office Action.

As regards independent Claims 40 and 45 see the rejection in this Office Action.

As regards Claims 3, 20, 23, 28, 33, 36, 44, 47 the *Eisenhofer–1* reference does not expressly disclose a checker.

The *Ly et al.* reference discloses a checker (Figure 1A, 5, 6, Col. 2 Lines 36-42).

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made, to have modified the *Eisenhofer–1* reference with the *Ly et al.* reference because diagnosing errors flagged by automatically generated checkers is much easier than diagnosing errors flagged by end-to-end tests, *(Ly et al. Col. 3 Lines 53-56).*

As regards Claim 7 the *Eisenhofer–1* reference does not expressly disclose a tree.

The *Ly et al.* reference discloses a process control tree (Figure 3A).

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made, to have modified the *Eisenhofer–1* reference with the *Ly et al.* reference because diagnosing errors flagged by automatically generated checkers is much easier than diagnosing errors flagged by end-to-end tests, *(Ly et al. Col. 3 Lines 53-56).*

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenhofer et al. U.S. Patent 6,108,494 hereafter referred to as the *Eisenhofer–1* reference in view of Worthington et al. U.S. Patent 5,881,270 and in further view of Eisenhofer et al. U.S. Patent 6,339,836 hereafter referred to as the *Eisenhofer-2* reference and in further view of Dearth et al. U.S. Patent 5,881,267.

As regards independent Claim 1 see the rejection in this Office Action.

As regards Claims 11 and 12 the *Eisenhofer–1* reference does not expressly disclose executing a remote procedure call.

The *Dearth et al.* reference discloses executing a remote procedure call (Col. 10 Lines 45-56).

It would have been obvious, at the time of the invention was made, to one of ordinary skill in the art to have modified the *Eisenhofer–1* reference with the *Dearth et al.* reference because the *Dearth et al.* reference discloses a method of improving the accuracy of a distributed simulation *(Dearth et al. Col. 3 Lines 30-35).*

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenhofer et al. U.S. Patent 6,108,494 hereafter referred to as the *Eisenhofer–1* reference in view of Worthington

et al. U.S. Patent 5,881,270 and in further view of Eisenhofer et al. U.S. Patent 6,339,836 hereafter referred to as the *Eisenhofer-2* reference and in further view of Dearth et al. U.S. Patent 5,732,247.

As regards independent Claim 1 see the rejection in this Office Action.

As regards Claim 19 the *Eisenhofer–1* reference does not expressly disclose handwritten test for all simulators.

The *Dearth et al.* reference discloses test written in a high-level language (Figure 1).

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to have modified the *Eisenhofer–1* reference with the *Dearth et al.* reference because the *Dearth et al.* reference discloses an improved method to write test routines for hardware simulation *(Dearth et al. Col. 2 Lines 14-20).*

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eisenhofer et al. U.S. Patent 6,108,494 hereafter referred to as the *Eisenhofer–1* reference in view of Worthington et al. U.S. Patent 5,881,270 and in further view of Eisenhofer et al. U.S. Patent 6,339,836 hereafter referred to as the *Eisenhofer-2* reference and in further view of Dearth et al. U.S. Patent 5,732,247.

As regards independent Claim 1 see the rejection in this Office Action.

As regards Claims 11 and 12 the *Eisenhofer–1* reference does not expressly disclose executing a remote procedure call.

The *Dearth et al.* reference discloses executing a remote procedure call that is deadlock safe (Figures 4, 4A, 4B, 4C, 4D).

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to have modified the *Eisenhofer–1* reference with the *Dearth et al.* reference because the *Dearth et al.* reference discloses an improved method to write test routines for hardware simulation *(Dearth et al. Col. 2 Lines 14-20).*

(10) Response to Argument

Appellant argues that the cited prior art references fail to teach or disclose the expressly disclosed limitation "*...operating each interface to convert the messages between a data format associated with the fixed configuration backplane and a data format associated with the simulator associated with the interface*".

On page 13 of Appellants' appeal brief is argued, *"However, the sections describing the simulators or their interfaces do not describe operating each interface to convert the messages between a data format associated with the fixed configuration backplane and a data format associated with the simulator associated with the interface as described in embodiments of the present application."*

The Examiner respectfully traverses Appellants' argument, *Eisenhofer-1* teaches a plurality of interfaces for each simulation module (Figure 2 items 241, 242, 243 and 244) and that data conversion, associated with the plurality of simulators and associated with the simulation backplane, takes place at the boundary between the simulator modules interface(s) and the simulation backplane ("In addition to synchronizing the simulators, the simulation backplane **210** also performs data type conversion...", Col. 12 lines 39-41), further *Eisenhofer-1* teaches ("Therefore, before transferring the signal state from the source simulator to one or more target simulators, signal mapping (also referred to as data type conversion) is performed between

the source and target representations in order to achieve consistent signal state representations...", Col. 12 lines 45-49) and finally, *Eisenhofer-1* teaches ("Mapping to intermediate simulation backplane types involves mapping from a data type associated with the source simulator to an intermediate abstract type associated with the simulation backplane **210** followed by mapping from intermediate abstract type to a data type associated with the target simulator...", Col. 12 lines 54-60).

On page 14 of Appellants' appeal brief is argued, *"However, as argued above, in embodiments of the present invention it is not the simulation backplane that performs a conversion messages between data format associated with the fixed configuration backplane and a data format associated with the simulator associated with the interface, but rather the interfaces associated with the simulators. Eisenhofer-1 does not describe such a limitation."*

Appellants' current claim language teaches, *"operating each interface to convert the messages between a data format..."* 10th line of independent claim 1, *Eisenhofer-1* teaches ("The simulator interfaces **241-244** each expose a standard set of interface routines for performing functions such as ...performing data type conversions...", Col. 5 lines 58-64). *Eisenhofer-1* teaches the simulator modules *performing* data type conversion. *Eisenhofer-1* also teaches data type conversions at the simulation backplane, ("In addition to synchronizing the simulators, the simulation backplane **210** also performs data type conversion...", Col. 12 lines 39-41).

On page 14 Appellants' argued, *"Therefore Eisenhofer-1 reference discloses performing data type conversion with a simulation backplane (possibly in conjunction with a user-programmable state translation table) in multiple embodiments"*

The Examiner agrees with this argument.

On page 15 of Appellants' appeal brief is argued, *"However, Applicants respectfully submit that none of the cited sections of Eisenhofer-1 teach, suggest or disclose"...operating each interface to convert messages between a data format associated with the fixed configuration backplane and a data format associated with the simulator associated with the interface" as specifically described in the embodiment of claim 1. Instead, as discussed above, the conversion between data types is accomplished with the use of the simulation backplane or s user-programmable state translation table in Eisenhofer-1."*

The Examiner respectfully traverses Appellants' arguments. *Eisenhofer-1* teaches ("The simulator interfaces **241-244** each expose a standard set of interface routines for performing functions such as ...performing data type conversions...", Col. 5 lines 58-64). *Eisenhofer-1* teaches the simulator modules *performing* data type conversion. *Eisenhofer-1* also teaches data type conversions at the simulation backplane, (Col. 12 lines 39-41 "In addition to synchronizing the simulators, the simulation backplane **210** also performs data type conversion...").

On page 15 of Appellants' appeal brief is argued, *"Eisenhofer-2 fails to make up for the deficiencies of Eisenhofer-1..."* The Examiner respectfully traverses Appellants' argument. *Eisenhofer-1* teaches ("The simulator interfaces **241-244** each expose a standard set of interface routines for performing functions such as ...performing data type conversions...", Col. 5 lines 58-64). *Eisenhofer-1* teaches the simulator modules *performing* data type conversion. Eisenhofer-1 also teaches data type conversions at the simulation backplane, ("In addition to synchronizing the simulators, the simulation backplane **210** also performs data type conversion...", Col. 12 lines 39-41).

Eisenhofer-2 is not required to teach Appellants' expressly claimed limitations because *Eisenhofer-1* teaches Appellants' expressly claimed limitations. Not withstanding this, *Eisenhofer-2* does teach Appellants' expressly claimed limitations and was provided in the rejections for that reason; see (Col. 11 lines 49-59) of *Eisenhofer-2.*

On page 15 of Appellants' appeal brief is argued, *"Worthington fails to support a proper §103(a) rejections for similar reasons...and does not disclose at least operating each interface to convert messages between a data format associated with the fixed configuration backplane as described in embodiments of the present application."*

The Examiner respectfully traverses Appellants' argument because *Eisenhofer-1* teaches Appellants' expressly claimed limitations. The Examiner stands by the combination of *Eisenhofer-1*, *Eisenhofer-2* and Worthington, for the reasons stated in the motivation to combine as provided in the Final Office Action dated, 4/6/2005 and included herein.

On page 15 of Appellants' appeal brief is argued, *"Similarly, Applicants submit there is no disclosure of operating each interface to convert the messages between a data format associated with the fixed configuration backplane in the Ly, Dearth-1, and Dearth-2 references as well."*

The Examiner respectfully traverses Appellants' arguments for reasons stated in this Examiner's Answer. *Eisenhofer-1* teaches Appellants' expressly claimed limitations.

On page 16 of Appellants' appeal brief is argued, *"Furthermore, Applicants submit that dependent claims 2-20, 22-25, 27-28, 30-33, 35-39, 41-44 and 46-50 are allowable as depending from allowable base claims."*

The Examiner respectfully traverses Appellants' argument and maintains the previously applied prior art rejections.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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